IN THE CLAIMS:

Claim 1 (cancelled).

2. (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of trench capacitors formed in said semiconductor substrate and arranged at a regular pitch;

a semiconductor layer formed on said semiconductor substrate in which said trench capacitors are formed;

an element isolation insulating film buried in said semiconductor layer to define a plurality of active element areas each spreading over two adjacent trench capacitors;

a plurality of transistors formed two by two in each of said plurality of active element areas, such that two transistors share one of source/drain diffusion layers, and the other of said source/drain diffusion layers is positioned over trenches of two adjacent trench capacitors, said transistors each having a gate connected to a word line continuous in one direction, each of said trenches of two adjacent trench capacitors is located under the gate of a corresponding transistor;

a first contact layer for connecting the other of said source/drain diffusion layers of each of said transistors to a capacitor node layer of corresponding one of said trench capacitors; ~~and~~

a bit line provided to intersect said word lines; and ~~connected to one of said source/drain diffusion layers of said transistor.~~

a second contact layer for connecting one of said source/drain diffusion layers to said bit line.

3. (Original) The semiconductor memory device according to claim 2, wherein said trench capacitors are each shaped substantially in a square having one side equal to 2F, where F is a minimum processing dimension, the diagonals of said squares are oriented in two orthogonal directions of said word line and said bit line, and said trench capacitors are arranged at a regular pitch of 1F or less in directions of two orthogonal sides of said squares.

4. (Original) The semiconductor memory device according to claim 2, wherein said trench capacitors are each shaped substantially in a square having one side equal to 2F, where F is a minimum processing dimension, the sides of said squares are oriented in two orthogonal directions of said word line and said bit line, and said trench capacitors are arranged at a regular pitch of 2F in the bit line direction, and shifted sequentially at a one-half pitch on adjacent bit lines.

5. (Original) The semiconductor memory device according to claim 3, wherein said active element areas are arranged at a regular pitch in said bit line direction and shifted sequentially by a one-quarter pitch on adjacent bit lines.

6. (Previously Amended) The semiconductor memory device according to claim 2, wherein said contact layer is buried such that said contact layer extends through the other of said source/drain diffusion layers to reach said capacitor node layer.

7. (Previously Amended) The semiconductor memory device according to claim 2, wherein:

said semiconductor layer comprises a first epitaxially grown layer and a second epitaxially grown layer formed on said first epitaxially grown layer;

said contact layer is formed such that said contact layer is buried in said first epitaxially grown layer to reach said capacitor node layer; and

the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer.

8. (Previously Amended) The semiconductor memory device according to claim 2, wherein said contact layer is formed such that said contact layer is buried in said semiconductor layer to reach said capacitor node layer, and the other of said source/drain diffusion layers is connected to said contact layer through a buried diffusion layer formed in an upper side portion of said contact layer.

9. (Previously Amended) The semiconductor memory device according to claim 2, wherein said contact layer is formed such that said contact layer is buried in said semiconductor layer to reach said capacitor node, and the other of said source/drain diffusion layers is connected to a top surface of said contact layer through a connection conductor formed on a surface thereof.

10. (Previously Amended) The semiconductor memory device according to claim 2, wherein:

said semiconductor layer comprises a bulk semiconductor layer of another semiconductor substrate bonded to said semiconductor substrate in which said capacitors are formed, and an epitaxially grown layer formed on said bulk semiconductor layer;

said contact layer is formed such that said contact layer is buried in said bulk semiconductor layer to reach said capacitor node layer; and

the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer.

11. (Original) The semiconductor memory device according to claim 10, wherein:

a substrate isolation insulating film is interposed on a bonding surface of said semiconductor substrate and said other semiconductor substrate bonded thereto;

said element isolation insulating film includes a first element isolation insulating film buried in element isolation regions in the bit line direction to a depth at which said first element isolation insulating film reaches said substrate isolation insulating film; and a second element isolation insulating film partially overlapping said first element isolation insulating film and buried in element isolation regions in the bit line direction and word line direction to a depth shallower than said first element isolation insulating film.

Cancel

12. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

an element isolation insulating film including a first insulating film buried to define active element areas ~~on~~ inside said semiconductor substrate, and a second insulating film shallower and wider than said first insulating film, said second insulating film buried inside said semiconductor substrate and positioned over the first insulating film; and

elements formed in said active element areas defined by said element isolation insulating film, said elements including a capacitor node formed in a trench in said semiconductor substrate, and a contact layer contacting an upper surface of said capacitor node, wherein said contact layer is formed in a contact hole in said semiconductor substrate.

Claims 13-17 (cancelled).

18. (Previously Amended) The device of claim 12, wherein said contact layer contacts an underside of second insulating film, and a side of the first insulating film.